

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-2003/0149943	08-2003	Yoshikawa, Atsushi	716/1
*	В	US-6,711,724	03-2004	Yoshikawa, Atsushi	716/6
*	С	US-6,341,363	01-2002	Hasegawa, Takumi	716/6
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	Δ	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Feehrer, "The Effect of Propagation Delay Uncertainty on the Speed of Time-of-Flight Digital Optoelectronic Circuits", Journal of Lightwave Technology, Vol. 14, No. 12, December 1996, pp. 2698-2713.
	V	Lee, "A Multilevel Parasitic Interconnect Capacitance Modeling and Extraction for Reliable VLSI On-Chip Clock Delay Evaluation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 4, April 1998, pp. 657-661.
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^{*}A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.